REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. Applicants would also like to thank the Examiner for correctly indicating as allowable the subject matter of dependent Claims 22-26, 29-30, 34-36, 39-40, 43-45, 48-49, 53-55 and 58-59.

Independent Claims 20, 31, 41 and 50 have been amended to more clearly define the present invention over the cited prior art references. The claim objections and claim informalities as helpfully noted by the Examiner have been addressed by amending the claims. In addition, the title has been changed to be more specific as requested by the Examiner, and noted grammatical errors in the specification have been corrected. The claim amendments and arguments supporting patentability of the claims are presented in detail below.

I. The Independent Claims Are Patentable

Independent Claims 20, 31, 41 and 50 have been rejected over the Faraboschi et al. patent in view of the Bratt et al. patent. Amended independent Claim 31 is directed to a processor for executing variable-sized instructions, with each instruction comprising up to N codes with N being a positive integer greater than 1. The processor comprises a memory comprising I individually addressable, parallel-connected memory banks with I being a positive integer at least equal to N. The memory comprises a program recorded in an interlaced fashion as a function of one code per memory bank and per address applied to the memory banks.

A reading circuit reads the memory by reading a code in each of the I memory banks during a cycle for reading an

instruction, with each instruction comprising a sequence of codes to be read and when a number of the sequence of codes of the instruction being read is less than I, then codes belonging to a following instruction are read.

Independent Claim 31 has been amended to recite that the reading circuit comprises an address circuit and a filtering circuit. The address circuit applies to the memory banks individual addresses generated from a collective value of a program counter that is incremented, before a beginning of the cycle for reading the instruction, by a value equal to a number of codes belonging to a previous instruction, and applies to each of the memory banks an individual read address that is based upon a result of a division by I of the collective value of the program counter. The filtering circuit filters codes that do not belong to the instruction to be read, while using parallelism bits accompanying the codes.

Independent device Claim 20 has been amended similar to independent device Claim 31 except the reading circuit, address circuit and filtering circuit have been replaced with reading means, address means and filtering means. Amended independent method Claim 41 is similar to amended independent device Claim 31. Amended independent method Claim 50 is similar to amended independent method Claim 41 except the step of providing a program memory is in the preamble of the claim instead of the body of the claim.

Referring now to the Faraboschi et al. patent, the Examiner cited Faraboschi et al. as disclosing a program memory comprising I individually addressable, parallel-connected memory banks, and a reading circuit for reading the program memory. The Examiner also cited Faraboschi et al. as

disclosing that the program memory comprises a program recorded in an interlaced fashion, and that the reading circuit reads a code in each of the I memory banks during a cycle for reading an instruction. When a number of codes of the instruction to be read is less than I, Faraboschi et al. discloses that codes belonging to a following instruction are read.

As correctly noted by the Examiner, Faraboschi et al. does not teach that the program recorded in the program memory is done so in an interlaced fashion as a function of one code per memory bank. The Examiner cited the Bratt et al. patent as disclosing this feature (col. 1, lines 29-64) of the present invention. The Examiner has taken the position that it would have been obvious to modify the processor in Faraboschi et al. to store consecutive instruction codes in consecutive memory banks in an interlaced fashion as a function of one code per memory bank, as disclosed in Bratt et al.

The Applicants respectfully submit that even if the references were combined as suggested by the Examiner, the claimed invention is still not produced. Faraboschi et al. discloses that an address circuit applies to each of the memory banks an individual read address generated from a collective value of a program counter that is incremented. Reference is directed to column 4, lines 25-30 of Faraboschi et al., which provides:

> "A program counter **200** provides successive instruction addresses of a program being executed to instruction cache **100** through an address buffer **202**. Instruction

> addresses are also provided to a cache refill state machine **204**, an adder **206** which increments program counter **200**, and to a comparator **208**." (Emphasis added.)

However, Faraboschi et al. fails to disclose that the address circuit applies to each of the memory banks an individual read address that is based upon a result of a division by I of the collective value of the program counter, as recited in the claimed invention. The Bratt et al. patent also fails to provide this noted deficiency.

Accordingly, it is submitted that amended independent Claim 31 is patentable over the Faraboschi et al. patent in view of the Bratt et al. patent. Amended independent Claims 20, 41 and 50 are similar to amended independent Claim 31. In view of the patentability of amended independent Claims 20, 41 and 50, it is submitted that the dependent claims which recite yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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